System Level Design Space Exploration of an Application Specific Wireless Sensor System

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Abstract

The advances in communication and computation technologies extend applicability of wireless sensor systems to new application domain. Although there are broad range of generic hardware platforms for wireless sensor networks (WSNs), the most of them developed on the commercial off-the-shelf (COTS) components and still cannot meet the requirements of certain target applications. Therefore, application specific or reconfigurable system-on-chip (SoC) hardware solutions are sometimes desirable. But producing chip takes time and is costly. Hence, it is extremely important to evaluate the ability of a new chip to meet the application domain requirements before the chip is physically available. This requires holistic approach to design and evaluate WSNs both in node and network levels.

1 Thesis statement

The technological advances behind WSNs give more possibilities to utilize them in many different application domains, resulting large design options of embedded hardware and software for wireless sensor systems. The existing design of sensor node hardware has appealing advantages in rapid deployment of a desired system in short time with low cost. The most of the state-of-the-art generic motes are designed by using the COTS components. They can be considered as the first generation of generic motes.

With the nanoscale semiconductor manufacturing techniques, not only processing and storage units of a computing device are integrated within a single chip also the communication and micro electromechanical parts can be build together. Such low-level implementation specific possibilities present new challenges in designing SoC hardware architectures for wireless sensor nodes. In order to improve timing performance and energy consumption, common domain-specific functions (i.e., data compression, error correction) start to be integrated to the processing unit as a hardware accelerator. Moreover, these accelerators are designed to be dynamically configurable depending on run-time application conditions. Designing an SoC hardware is complex, takes time and is costly. So, if hardware is still in its design flow, it is extremely important to evaluate the ability of a new chip to meet the application domain requirements before the chip is physically available. The objective of this thesis is to propose a methodology/tool that can evaluate the alternative designs of wireless sensor system based on SoC hardware, while the hardware is still in its design flow.

2 Problem domain

The main problem is how to evaluate system-wide performance of application specific wireless sensor system based on generic SoC hardware, where hardware is still at the early stages of design. Like most embedded systems, WSNs include both hardware and software components specialized to a target application domain. The most common methodologies used for system-wide performance analysis are to use component specific simulators separately and manually carry out performance analysis. Such time-consuming tasks can deliver sub-optimal solutions because global, cross-layer optimizations are difficult. So the main problems that must be addressed within this thesis are:

- re-use of the good hardware and software platforms from the appropriate design space to narrow down solution space (TinyOS [5], SoC)
- abstract whole system in different levels (node and network) by separating functional behavior and implementation solution
- represent different design aspects in the common form (modeling)
- carry out performance analysis in reasonably easy way with less cost (hierarchical simulations with different accuracy granularity)

Expected contributions are:

- system-level design space exploration of wireless sensor systems
- integration of VLSI circuit design flow
- executable system models of WSNs, specific to the certain application domain

3 Related work

For the system-level design and verification of wireless sensor systems, certain tools are being used in the research community.

Viptos [2, 3], a Ptolemy II-based framework [1], supports the actor-oriented modeling and design concept [7], a rich set of the execution semantics for different domains, graphical visualization and TinyOS/TOSSIM integration. Sensor nodes, wireless communication channels and physical medium can be defined by creating composite models using Ptolemy II basic models or directly in Java or other programming languages. Hence, it enables developers to share models that represent disjoint aspects of the WSNs and to construct models that include sophisticated elements from several aspects. The known limitations on Viptos are its simulation support only for the Mica motes and increase in simulation time linearly proportional to number of nodes in a model.

COOJA [10], cross-layer simulator, enables simultaneous simulation at several layers. It represents high-level application functionality in Java, integrates execution of TinyOS or Contiki native codes and supports Java-based emulator. Sensor node hardware platforms, operating system specific software applications, radio propagation models are all considered and can be changed or replaced.

Both of these existing tools for design and verification of WSNs focus on the COTS platforms and portable sensor network software, like TinyOS or Contiki. None of them is applicable to SoC design flow.

4 Methodological approach

Abstracting a system in alternative forms that ease capturing properties and behaviors of different aspects of a system for analysis is the main focus of the electronic system-level design. Our approach is relied on modeling properties that can represent whole system in hierarchical levels of abstraction. Here, the actor-oriented principle is used to represent wireless sensor systems, while it can hierarchically abstract complete system by mixing well-defined models of computation. By utilizing appropriate models of computation, we could perform simulations for performance analysis at two different abstraction levels, namely network and node levels. With its polymorphic modeling capabilities, the Ptolemy II framework was chosen as a basis tool in our work.

At the network level, templates of sensor platforms will be defined and implemented as actors. These templates are actually behavioral simulation models and abstract sensor node platform. Also, the important application specific aspects, such as sensor node mobility will be considered at the network level.

At the node level, cycle-accurate (VHDL) model of the main computation module (processor + storage) of a target hardware platform will be examined. The deterministic timing and power dissipation characteristics of the widely used radio transceiver modules can be a good reference for a generic transceiver model, which might also be implemented as an actor.

The interface between the node and network levels will be a sensor operating system, in our case it is TinyOS. Its modular structure, component classification, simulation and debug support are best fit to our approach. Performance evaluation criterion/metrics such as energy consumption or power dissipation, delay or latency, and node connectivity will be defined at both levels and correlations or dependencies between them will be determined.

The system-wide performance evaluation will be done in three steps. First, with system simulations on the network models reasonably accurate performance estimates can be obtained. Next, based on these estimates, cycle-accurate simulations on the node models are performed to investigate the estimates in details. Finally, results from the low-level simulations are analyzed and optimization suggestion for particular design issue will be made.

5 Research results

Within the scope of the proposed research work following results have been achieved so far.

5.1 Node level abstraction

As a target hardware an SoC architecture based on a dynamically reconfigurable processor was chosen [6]. The processing unit of the architecture consists of a 32-bit LEON2 processor [4], which is the single threaded, SPARC-compliant RISC processor. A dynamically reconfigurable function unit (RFU) is directly added into the processors instruction pipeline so that it can process the predefined computational-intensive tasks with minimal processor intervention. This SoC architecture is described in synthesizable VHDL.

In order to abstract the chosen sensor node architecture the TinyOS sensor network operating system was ported [8]. The required hardware specific and system related components that are necessary to any basic TinyOS applications have been implemented and tested by using both the hardware simulator (ModelSim) and FPGA-based prototyping boards. The compilation analyses showed that the amount of required memory is still within the range that the most existing generic sensor node platforms have. In order to test the TinyOS porting and track software execution during simulation, an additional monitoring tool has been developed and integrated to the hardware simulator. The monitoring tool facilitates software tracing on cycle-accurate simulation of any LEON2 processor based SoC design.

5.2 Network level abstraction

System-level executable platform template of our target hardware is modeled on the basis of Viptos framework. The work mainly has been done in this part is the implementation of the TOSSIM simulation components and actor-oriented definitions for the SoC based sensor node.

The essential simulation components, like clock, interfaces to timer and I/O, were added to the TOSSIM library and validated with TOSSIM simulations.

For a platform template definition, which will basically abstract the target hardware, the description of the predefined prototyping board from [8] was directly used. The platform template was described in MoML, the primary persistent file format to represent models in Ptolemy II, and includes the actor-oriented definition of the hardware interfaces to the LEON2-based SoC architecture and LEDs, the XML definitions of the I/O ports for UART, LEDs and radio. In order to couple TinyOS applications to the platform template, the transformation tools included in Viptos were utilized with some modification. The main component of Ptolemy II, which communicates with the TOSSIM simulation engine, was also modified. The successful simulation of a small network model containing platform templates built on the target SoC architecture has been validated the whole modeling and transformation flow.

5.3 Application specific models

A wildlife tracking and monitoring application was chosen as a target application, because it has many interesting challenges. The most important requirements are: cost, lifetime, form factor, and connectivity. If animals under study will be equipped with sensor nodes, their movement introduces mobility to a network. A balance between energy efficiency and reliable network connectivity can be reached when behavior of the target, particularly the movement pattern of the studied animals, is taken into account in system modeling and performance evaluation. Hence, a proper mobility model is an important issue in our work.

A group mobility model is implemented as an application specific model [9]. The model is parameterable and can present individual and group motion according to the specified distributions of moved distance and turning angle, which mainly describe animal movement. In order to be matched the basis system-level modeling and verification framework for WSNs, the mobility model is implemented accordingly to the actor-oriented modeling concept. Therefore, this mobility model is independent of any sensor system design and can be used in arbitrary system model to present certain application scenarios.

6 Work to be done

The following work is need to be done and is still open to discussion.

- define performance metrics and mechanism to evaluate performance (i.e., use application profiling technique)
- collect performance results from simulation, prototypes or motes, refine platform template
- define optimization strategy, evaluate it

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